ABSTRACT OF THE DISCLOSURE

A system for measuring timing margins in an interface between a core and an input/output device on a chipset. In order to measure the amount of available variation in data and strobe signals, delay lines are introduced so that the data and strobe signals may be varied in relation to each other. By incrementally changing the delay and hence the time difference between the two signals, it is possible to determine the allowable variation when the device fails to operate. By providing delays on both sides, it is possible to determine the timing margin on both the setup and hold of the signals.